**Amendments to th Specification**

Please amend line 21 of page 4 to read the following:

FIG. 7~~A~~ is a graph illustrating a change in an output clock signal over time; and

Please amend line 22 of page 4 to read the following

FIG. 8 ~~7B~~ is a graph illustrating a change in an output duty cycle with respect to a change in an input duty cycle.

Please amend paragraph 1 of page 5 to read the following:

FIG. 3 is a circuit diagram of a digital duty cycle correction circuit for a multi-phase clock according to an embodiment of the present invention, FIG. 4 is a circuit diagram of a digital duty cycle detection circuit of the digital duty cycle correction circuit of FIG. 3, FIG. 5 is a circuit diagram of a current integrator used in the digital duty cycle detection circuit of FIG. 4, FIG. 6 is a timing diagram of the digital duty cycle detection circuit, FIG. 7~~A~~ is a graph illustrating a change in an output clock signal over time, and FIG. 8 ~~7B~~ is a graph illustrating a change in an output duty cycle with respect to a change in an input duty cycle.

Please amend paragraph 3 of page 7 to read the following:

FIG. 7~~A~~ is a graph obtained by simulating a procedure of duty cycle correction of an input clock signal with a frequency of 1.25GHz in which the phase of the rising edge of the input clock is held constant and only the phase of the falling edge of the input clock is not held constant. The characteristic illustrated by FIG. 7~~A~~ makes it possible to perform duty cycle correction without changing the phase of a multi-phase clock signal.

Please amend paragraph 4 of Page 7 to read the following:

FIG. 8 ~~7B~~ shows a simulation result of a change in the duty cycle of an output clock signal with respect to a change in the duty cycle of an input clock signal. Referring to FIG. 8 ~~7B,~~ the digital duty cycle correction circuit according to the present invention can operate over a large range (about 15% - 85% duty cycle for an input clock signal with a frequency of 1.25GHz) without being largely affected by the duty cycle of the input clock signal if a duty cycle (about 15% duty cycle for an input clock signal with a frequency of

1.25GHz) enables detection of the rising edge of the input clock. Also, since the digital duty cycle correction circuit corrects the duty cycle in a digital manner, a corrected duty cycle is held constant within an operating range.